CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A phase locked loop for open loop mode, comprising:

a voltage controlled oscillator having a first tuning input for a tuning voltage and a signal output for an output signal of tunable frequency;

said voltage controlled oscillator having a frequency-determining capacitance controlled using a second tuning input;

a frequency divider having an adjustable division ratio for the purpose of channel adjustment for the phase locked loop, having an input coupled to said signal output of said voltage controlled oscillator, having an output carrying a frequency-divided output signal and coupled to said first tuning input of said voltage controlled oscillator in a control loop, and having a control input for stipulating the division ratio;

a loop filter having a memory effect;

a phase detector having a first input connected to said output of said frequency divider, a second input connected to a reference frequency source, and an output connected via said loop filter to said first tuning input of said voltage controlled oscillator; and

a frequency stipulation unit for programming the frequency of the output signal of tunable frequency connected, firstly, to said control input of said frequency divider for transmitting a frequency word and, secondly, to said second tuning input of said voltage controlled oscillator for transmitting the frequency word such that a change in the tuning voltage upon a change in the frequency word disappears or is as small as possible in order to avoid any frequency drift in an open loop mode of the phase locked loop;

said voltage controlled oscillator having resonant frequency preselection to compensate for the memory effect of said loop filter.

Claim 2 (canceled).

Claim 3 (currently amended). The phase locked loop according to claim 1, wherein said frequency-determining capacitance is a controllable capacitance formed by a variable capacitance diode.

Claim 4 (currently amended). The phase locked loop according to claim 1, wherein said frequency-determining capacitance is a controllable capacitance comprising a plurality of discrete capacitor elements each to be selectively connected or disconnected.

Claim 5 (currently amended). The phase locked loop according to claim 4, wherein said plurality of discrete capacitor elements are graded on a binary basis.

Claim 6 (currently amended). The phase locked loop according to claim 1, which further comprises a digital/analog converter connected between said frequency stipulation unit and said second tuning input for driving said frequency-determining capacitance with the frequency word from said frequency stipulation unit.

Claim 7 (currently amended). The phase locked loop according to claim 6, wherein said frequency-determining capacitance is a controllable capacitance formed by a variable capacitance diode driven by said frequency stipulation unit.

Claim 8 (currently amended). The phase locked loop according to claim 1, which further comprises a data bus connecting

said frequency stipulation unit to said control input of said frequency divider and to said second tuning input of said voltage controlled oscillator for transmitting the frequency word.